Datasheet

BMP561

Arm® Cortex® -M0+ Core-based 32-bit MCU

Version: V1.2

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1 Product Characteristics

Core

- 32-bit Arm® Cortex® -M0+ core
- Up to 4MHz working frequency
- AHB and APB Bus

Memory

- Main Flash: 64KB
- Data Flash: 4KB
- SRAM: 8KB

Clock

- HSICLK: 4MHz high-speed internal RC oscillator
- LSICLK: 65.536kHz low-speed internal RC oscillator

Power Supply and Reset

- Supply voltage range: 2.0V~5.5V
- Low-dropout (LDO) regulator
- Support system reset and power reset

Work Mode

- Support Normal, Sleep, DeepSleep, and Hibernate modes
- Support WAIT, SLEEP, DPSLEEP, HIBERNATE, ACTIVE, and OFF status

GPIO

- Provide up to 9 I/O interfaces
- All I/O interfaces can be mapped to external interrupt vectors

Communication Peripherals

- 1×I2C
- 1×UART

Analog Peripherals

- 1×16-bit C-ADC for current sampling
- 1×16-bit V-ADC for voltage sampling

Timer

- 2×16-bit timers TMR0/1 provide PWM output
- 2×watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
- 1×internal wake-up timer WUPT
- 1×24-bit decrementing system tick timer

Algorithm

- Hash algorithm SHA256

Chip Package

- WLCSP12
- DFN12
- QFN16

Contents

2 Product Information

See the following table for BMP561 product functions and peripheral configuration.

Table 1 Functions and Peripherals of BMP561 Series Chips

Product		**BMP561**		
Model		Y8Y6	Y8D6	L8U6
Package		WLCSP12	DFN12	QFN16
Core and maximum operating frequency		Arm® Cortex®-M0+@4MHz		
Working voltage		2.0V~5.5V		
Main Flash (KB)		64		
Data Flash (KB)		4		
SRAM (KB)		8		
GPIOs		5	5	9
Communication interface	I2C	1		
	UART	1		
Timer	16-bit advanced timer	2		
	System tick timer	1		
	Watchdog	2		
	18-bit WUPT	1		
16-bit C-ADC		1		
16-bit V-ADC		1		
Operating temperature		Ambient temperature: −40°C to 85°C Junction temperature: −40°C to 105°C		

3 Pin Configuration and Functions

3.1 Pin Distribution

Figure 1 WLCSP12 Top View

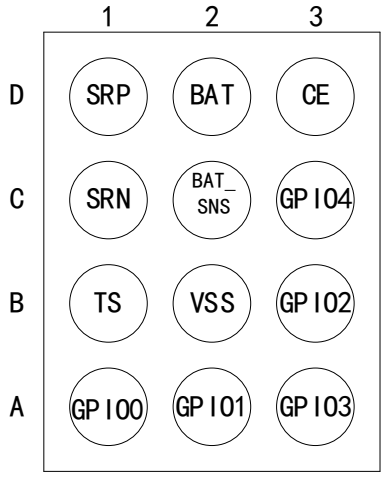


Figure 2 DFN12 Top View

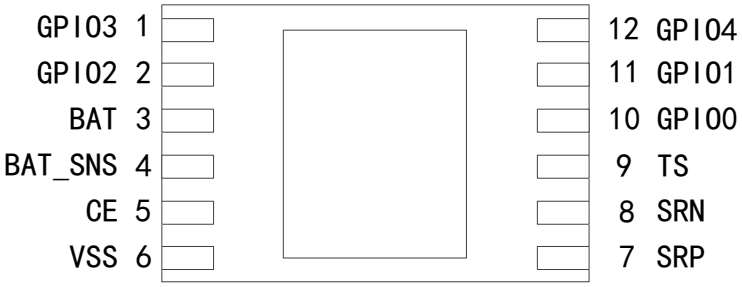
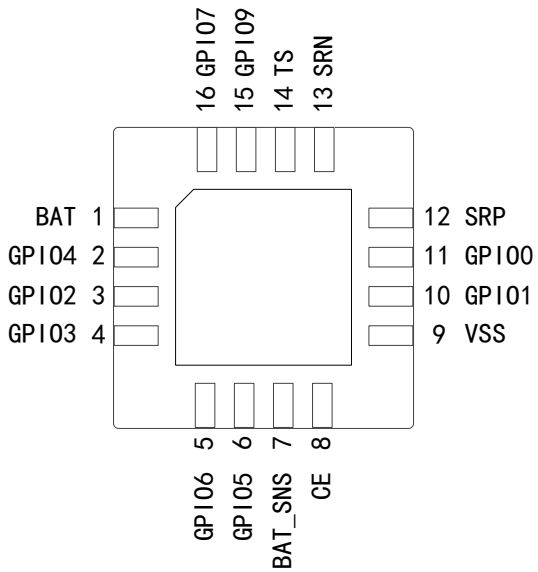


Figure 3 QFN16 Top View



3.2 Pin Functions

Table 2 Abbreviations for Pins

Name		Abbreviations	Definitions
Pin name		Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power supply pin
		I	Only input pin
		O	Only output pin
		AI	Analog input pin
Pin function	Default multiplexing function	Select/enable this function directly through peripheral register	
	Redefining function	Select this function through AFIO remapping register	

Table 3 Pin Functions

NAME	Multiplexing	TYPE	DESCRIPTION	WLCSP12	DFN12	QFN16
GPIO0	INT0, TMR0OUT, TXD	I/O	SWDIO	A1	10	11
GPIO1	INT1, TMR1OUT, RXD	I/O	SWCLK	A2	11	10
GPIO2 (SCL)	-	I/O	I2C Serial Clock	B3	2	3
GPIO3 (SDA)	-	I/O	I2C Serial Data	A3	1	4
GPIO4	INT2, SYS_CLK	I/O	GPIO4	C3	12	2
TS	-	AI	External temperature sensor input	B1	9	14
VSS	-	P	Ground	B2	6	9
SRN	-	AI	Analog input pin connected to internal C-ADC	C1	8	13
BAT_SNS	-	AI	Battery Sense	C2	4	7
SRP	-	AI	Analog input pin connected to internal C-ADC	D1	7	12
BAT	-	P	Battery measurement input	D2	3	1

NAME	Multiplexing	TYPE	DESCRIPTION	WLCSP12	DFN12	QFN16
CE	-	I	Chip enable signal, valid with high level	D3	5	8
GPIO5	-	I/O	GPIO5	-	-	6
GPIO6	-	I/O	GPIO6	-	-	5
GPIO7	-	I/O	GPIO7	-	-	16
GPIO9	-	I/O	GPIO9	-	-	15

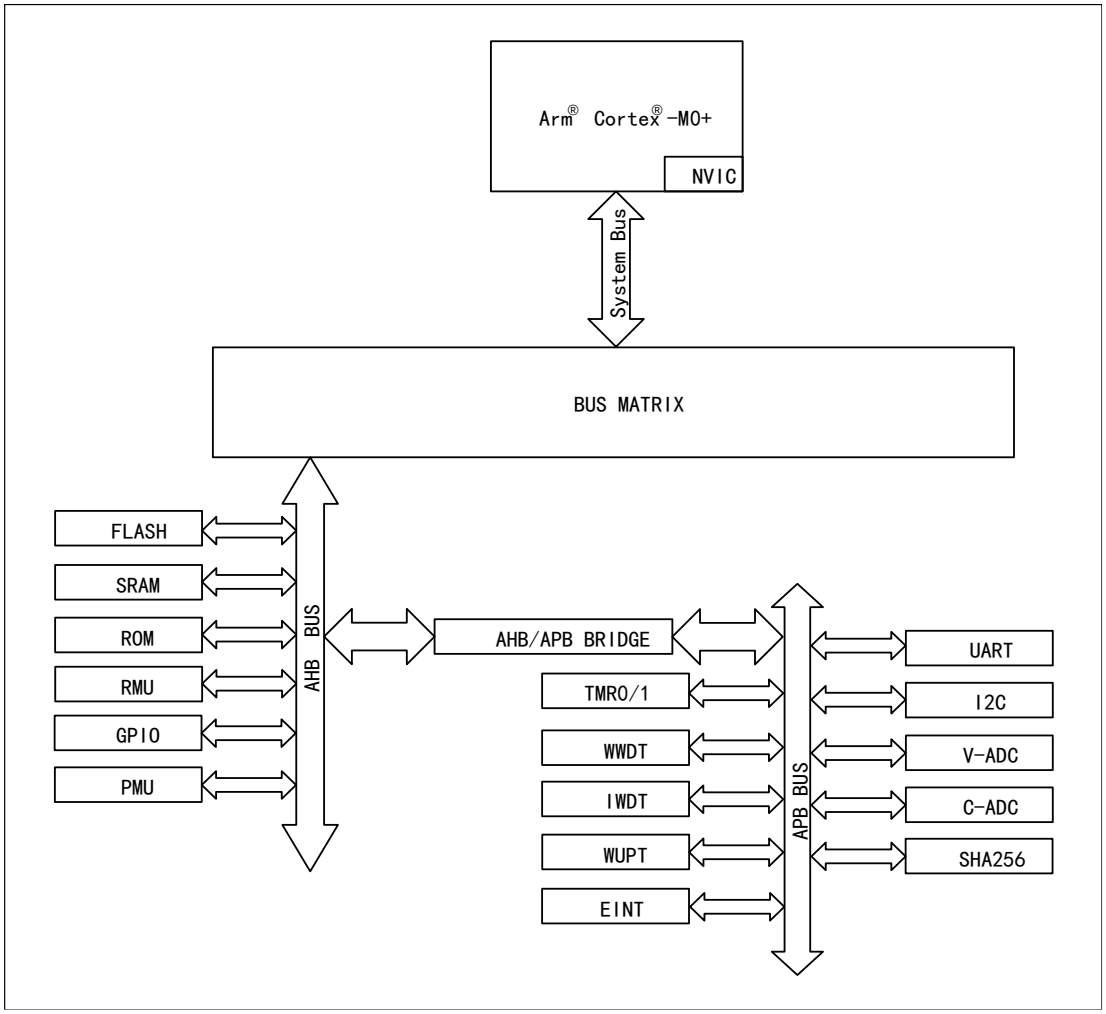
4 Functional Description

This chapter mainly introduces the system architecture, interrupts, on-chip memory, clock, power supply, and peripheral features of the BMP561 products. For information related to the Arm® Cortex®-M0+ core, refer to the Arm® Cortex®-M0+ Technical Reference Manual, which can be downloaded from the Arm company's website.

4.1 System Architecture

4.1.1 System Block Diagram

Figure 4 System Block Diagram



4.1.2 Address Mapping

The total memory-mapped address is 4GB, and the allocated addresses include the core (including core peripherals), on-chip Flash (including main storage area, system storage area, and option bytes), on-chip SRAM, and bus peripherals (including AHB and APB peripherals).

Table 4 Address Mapping

Area	Start Address	Name of Peripherals
-	0x0000 0000	Reserved
AHB Bus	0x0002 0000	ROM
AHB Bus	0x0002 3000	Reserved
AHB Bus	0x0800 0000	Main FLASH
AHB Bus	0x0801 0000	Data FLASH
AHB Bus	0x0801 1000	Option Bytes & Reserved
-	0x0801 2000	Reserved
AHB Bus	0x2000 0000	SRAM
-	0x2000 2000	Reserved
APB Bus	0x4000 0000	I2C
APB Bus	0x4000 1000	Reserved
APB Bus	0x4000 2000	UART
APB Bus	0x4000 3000	IWDT
APB Bus	0x4000 4000	WWDT
APB Bus	0x4000 5000	TMR0
APB Bus	0x4000 6000	TMR1
APB Bus	0x4000 7000	C-ADC
APB Bus	0x4000 8000	V-ADC
APB Bus	0x4000 9000	WUPT
APB Bus	0x4000 A000	SHA256
APB Bus	0x4000 B000	EINT
APB Bus	0x4000 C000	Reserved
APB Bus	0x4001 0000	SYSCTRL
APB Bus	0x4002 0000	FLASH
APB Bus	0x4003 0000	GPIO
APB Bus	0x4004 0000	Reserved
-	0x5000 0000	Reserved
Cores	0xE000 0000	Core Peripherals

4.2 Core

The BMP561 features an Arm® Cortex®-M0+ core, which is developed for low cost and low power consumption, providing excellent computing performance

and advanced system interrupt response, and including compatibility with all Arm tools and software.

4.3 Flash

The chip has embedded 64KB Main Flash, 4KB Data Flash, and 8KB SRAM, enabling storage of instructions and data. It supports 32-bit data read and write access, along with low power modes and security protection features.

4.4 Clock

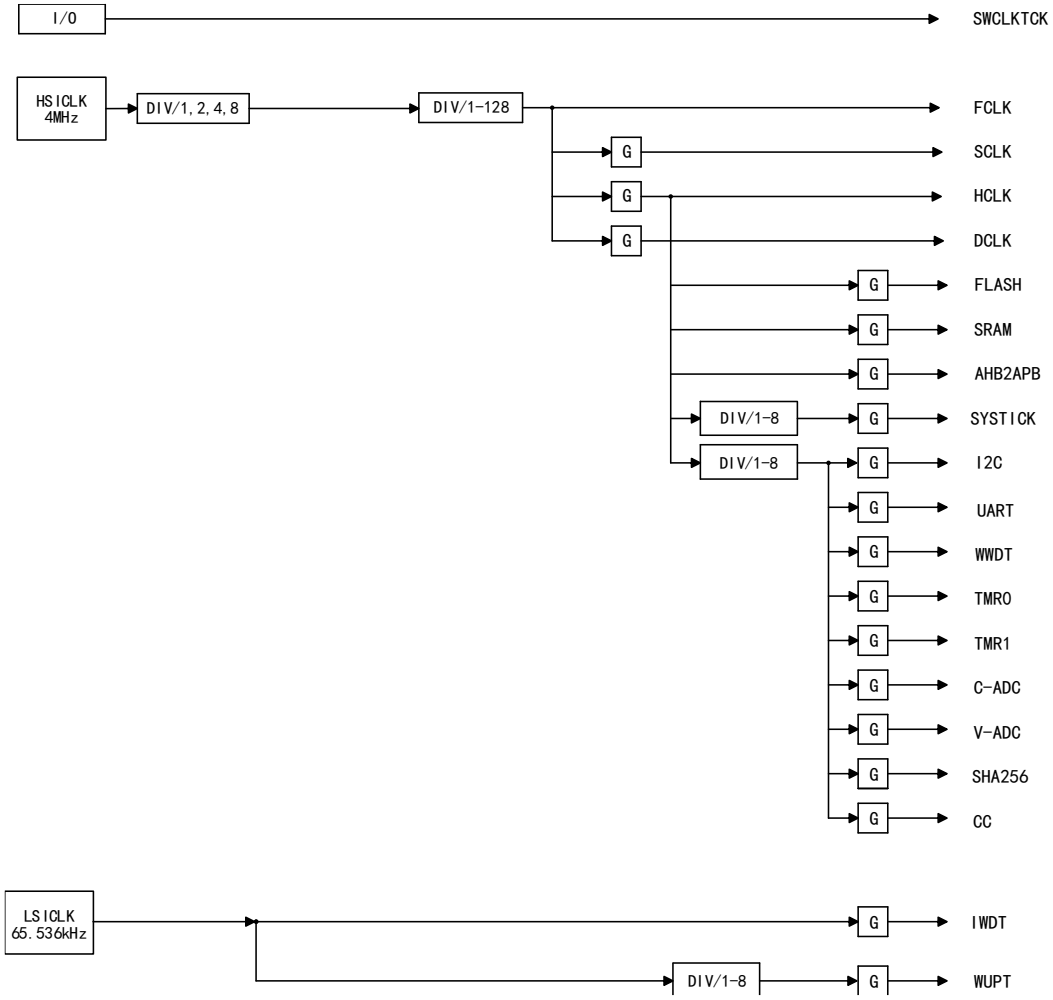
4.4.1 Clock Source

Two different clock sources are used to drive the system clock:

- HSICLK: 4MHz internal RC oscillator
- LSICLK: 65.536kHz internal RC oscillator

4.4.2 Clock Tree

Figure 5 Clock Tree



Note: G stands for gate, which is used to turn the clock on and off.

4.5 Interrupt Controller

4.5.1 Nested Vector Interrupt Controller (NVIC)

The NVIC can handle up to 23 maskable interrupt channels (excluding the 16 interrupt lines of the Arm® Cortex®-M0+) and 4 priority levels. The tightly coupled NVIC interface can directly pass the interrupt vector entry address to the core, achieving low-latency interrupt response handling. In addition, it prioritizes high-priority interrupts, automatically saves the processor state, and restores it upon interrupt return without additional instructions. This module provides flexible interrupt management with minimal interrupt latency.

4.5.2 External Interrupt Controller (EINT)

The EINT consists of 3 interrupt request level and edge detectors, which can be configured to GPIO ports. Each input line can be independently configured for input type (level or edge) and can be independently enabled. The pending register holds the interrupt request status from the input lines.

4.6 Reset

The chip has two types of reset methods: system reset and power reset.

- System reset resets the register to the reset state. A system reset occurs when a window watchdog event, independent watchdog event, software reset, or upload reset happens.
- Power reset occurs during power-on, power-down, low-voltage reset, or when exiting from HIBERNATE state.

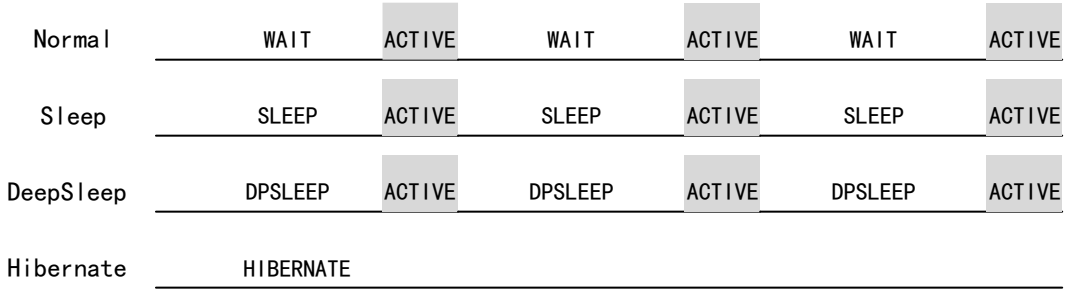
4.7 Power Management

Power supply is the foundation for the stable operation of a system, and the operating voltage of the chip is 2.0V to 5.5V.

The chip supports the following operating modes: Normal, Sleep, DeepSleep, and Hibernate.

The chip supports the following low-power states: WAIT, SLEEP, DPSLEEP, and HIBERNATE. The normal state is ACTIVE, while the non-working state is OFF.

Figure 6 Operating Modes



Different operating modes consist of different working states:

- Normal mode: composed of WAIT and ACTIVE states.
- Sleep mode: composed of SLEEP and ACTIVE states.
- Deep Sleep mode: composed of DPSLEEP and ACTIVE states.
- Hibernate mode: always in HIBERNATE state.

4.8 GPIO

Embedded with 9 GPIO pins. Pin input can be configured as pull-up/pull-down, floating, or analog, while pin output can be configured as pull-up/pull-down, push-pull, or open-drain. Most GPIO pins are shared with multiplexed peripherals. Additionally, some pins have redefined functions, such as analog input, external interrupt, and input/output for chip peripherals. However, only one function can be mapped to a pin at any given time. The remapping of multiplexing functions can be achieved through controlling the option bytes.

4.9 Timer

There are two identical timers, TMR0 and TMR1, which operate independently. The counter module features a 16-bit programmable prescaler and a 16-bit up counter, while also supporting one PWM output.

4.10 Watchdog

The watchdog is divided into independent watchdog (IWDT) and window watchdog (WWDT):

- The independent watchdog has its own clock source and monitors the system's operational status. It is suitable for environments that require independence but do not have high accuracy demands. Even in the event of a main clock failure, the independent watchdog remains effective and can be used to wake the system from Sleep mode.
- The window watchdog is suitable for situations that require precise timing, detecting software failures, and abnormal application behavior. The clock for the window watchdog comes from PCLK, and the counter

clock is derived from the CK counter clock through prescaling. If the window watchdog does not receive a feed operation within the time period set by the program, it will generate a reset signal.

4.11 WUPT

When the MCU enters a low power state (WAIT/SLEEP/DPSLEEP), the wake-up controller provides an internal wake-up time reference. The clock for this time reference is supplied by the internal low-speed RC oscillator clock (LSICLK).

4.12 Communication Peripherals

4.12.1 I2C

There is one embedded I2C interface, which is externally connected via the data pin (SDA) and the clock pin (SCL). It can enable or disable interrupts. It operates in slave mode, supporting 7-bit addressing, and allows connection to standard (up to 100 kHz) or fast (up to 400 kHz) I2C buses. I2C supports both receiving and transmitting data, converting serial data into parallel data when receiving, and converting parallel data into serial data when transmitting.

4.12.2 UART

UART is a serial communication device that can flexibly perform full-duplex and half-duplex data exchange with external devices. It features an embedded UART communication interface with independent full-duplex transmit and receive channels, a programmable baud rate generator, configurable parity enablement, and STOP bits.

4.13 ADC

BMP561 consists of two ADC controllers: one C-ADC and one V-ADC.

4.13.1 C-ADC

C-ADC is a 16-bit Σ-Δ analog-to-digital converter for current sampling, with the reference voltage V_{ref} generated by V_{DD}.

The CADCEN signal controls the enabling of C-ADC. After the RSTN signal is released, the C-ADC reset is completed, and it starts conversion. The SP_DONE signal indicates the end of the conversion. Once the conversion is finished, the C-ADC data register is updated, and an interrupt is generated (if C-ADC interrupts are enabled).

C-ADC converts the signals at the SRP/SRN input terminals, and the conversion results are placed in the C-ADC register.

4.13.2 V-ADC

V-ADC is a 16-bit Σ-Δ analog-to-digital converter for voltage sampling. The reference voltage V_{ref} is generated by V_{DD} and provides multiple ADC input channels selection.

The VADCEN signal controls the enabling of V-ADC. After the RSTN signal is released, the V-ADC reset is completed, and it starts conversion. The SP_DONE signal indicates the end of the conversion. Once the conversion is completed, the V-ADC data register is updated, and an interrupt is generated (if V-ADC interrupts are enabled).

V-ADC provides an automatic conversion feature, allowing certain channels to switch automatically, completing the required delay, and generating an interrupt only after all data testing is completed.

4.14 SHA256

The SHA256 algorithm is a classic hash algorithm that can convert data of arbitrary length into fixed-length data. The SHA256 algorithm has strong collision resistance and is irreversible. It can be applied in areas such as data signing, data consistency, privacy protection, and user password protection.

5 Electrical Characteristics

5.1 Test Conditions

5.1.1 Maximum and Minimum Values

Unless otherwise specified, all products are tested on the production line at T_A=25°C. The maximum and minimum values support the specified worst-case environmental temperature, supply voltage, and clock frequency.

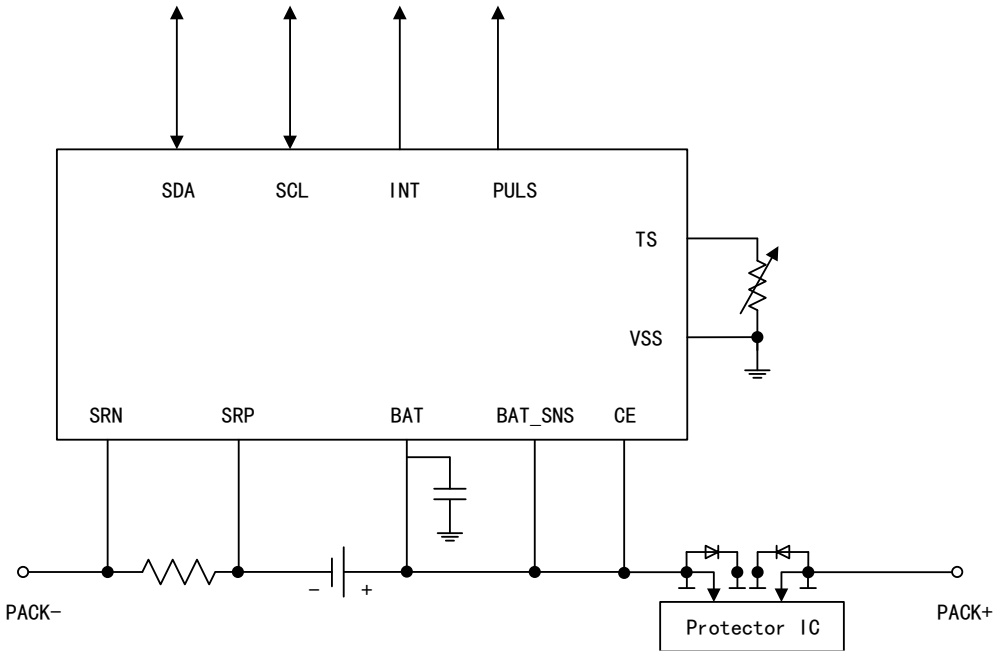
Notes below each table indicate that the data is obtained through comprehensive evaluation, design simulation, or process characteristics and has not been tested on the production line. Based on comprehensive evaluation, the maximum and minimum values are obtained by sample testing, taking the average and adding or subtracting three times the standard deviation (average±3Σ).

5.1.2 Typical Values

Unless otherwise specified, the typical data is measured at T_A=25°C and V_{BAT}=3.6V, and these data are provided for design guidance only.

5.1.3 Power Supply

Figure 7 Power Supply



5.2 Absolute Maximum Ratings

Table 5 General Operating Conditions[1]

Symbol	Parameter	Minimum value	Maximum value	Unit
V_{BAT}	Battery input voltage	–0.3	6	V
V_{CE}, V_{GPIOx}	Input/Output pin voltage	–0.3	6	
V_{SRP}, V_{SRN}, V_{BAT_SNS}	V_{SRP} and V_{SRN} are the positive and negative input voltages of the C-ADC. V_{BAT_SNS} is the sampling point of V_{BAT}, sent to V-ADC	–0.3	V_{BAT}+0.3	
V_{TS}	Temperature sensor voltage	–0.3	2.1	
V_{SCL}, V_{SDA}	Communication pin voltage	–0.3	6	
T_A	Ambient temperature	–40	85	°C
T_J	Junction temperature	–40	125	
T_{stg}	Storage temperature	–65	150	

Note: [1] Unless otherwise specified, the data is obtained under operation within the normal temperature range. Stresses listed above the absolute maximum ratings may cause permanent damage to the device. These are stress value limits and do not imply that the device will operate normally under these or any other conditions beyond the recommended operating conditions. Prolonged exposure to absolute maximum rated conditions may affect the reliability of the device.

5.3 ESD

Table 6 ESD Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A=24°C, compliant with ANSI/ESDA/JEDEC JS-001-2023	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A=24°C, compliant with ANSI/ESDA/JEDEC JS-002-2022	2000	

Note: [1] Tested by a third-party testing agency, not tested in production.

5.4 Latch-up

Table 7 Latch-up[1]

Symbol	Parameter	Condition	Type
LU	Latch-up	T_A=125°C, compliant with JESD78F.02-2023	Class Ⅱ A

Note: [1] Tested by a third-party testing agency, not tested during production.

5.5 Recommended Operating Conditions

Table 8 Recommended Operating Conditions[1]

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{BAT}	Battery input voltage	2.0	-	5.5	V
C_{BAT}	External capacitor from BAT to VSS	1	-	-	μF
V_{TS}	Temperature sensor voltage	0	-	1.5	V
V_{GPIOx}, V_{CE}	Input/Output pin voltage	0	-	V_{BAT}	
V_{SCL}, V_{SDA}	Communication pin voltage	0	-	V_{BAT}	

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.6 Thermal Information

Table 9 Thermal Information[1][2]

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	120.5	°C /W
$R_{\theta JC(top)}$	Junction to case (top) thermal resistance	0.25	
$R_{\theta JB}$	Junction to board thermal resistance	43	
Ψ_{JT}	Junction to top characterization parameter	3.25	
Ψ_{JB}	Junction to board characterization parameter	42.25	
$R_{\theta JC(bot)}$	Junction to case (bottom) thermal resistance	-	

Note:

[1] Unless otherwise specified, data is obtained under normal temperature conditions.

[2] For more information on traditional and new thermal information, see the Semiconductor and IC Package Thermal Metrics Application Report (SPRA953).

5.7 Supply Current

Table 10 Supply Current[1]

Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
I_{ACTIVE}	Standard operating conditions	-	60	-	μA
I_{SLEEP}	Sensor resistor current below SLEEP threshold	-	18	-	
$I_{DPSLEEP}$	Sensor resistor current below DPSLEEP threshold	-	8	-	
I_{OFF}	CE=V_{IL}	-	0.5	-	

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.8 Internal 1.5V LDO

Table 11 Internal 1.5V LDO[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REG18}	LDO output voltage	-	1.35	1.5	1.65	V
V_{PORhy}	POR hysteresis	-	-	0.05	-	

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.9 I/O Information（CE, GPIOx）

Table 12 I/O Information（CE, GPIOx）

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IH}	High-level input voltage	V_{LDO}=1.5V	0.7 V_{BAT}	-	-	V
V_{IL}	Low-level input voltage	V_{LDO}=1.5V	-	-	0.3 V_{BAT}	
V_{OL}	GPIOx low-level output voltage	V_{LDO}=1.5V, I_{OL}=1mA	-	-	0.4	

5.10 Internal Oscillator Specifications

Table 13 Internal Oscillator Specifications[1]

Clock	Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
HSICLK	f_{HSICLK}	Operating frequency	-	-	4	-	MHz
	f_{HSICLK_DRIFT}	Frequency drift	T_A=−20°C~65°C	−1.8	-	4.5	%
			T_A=−40°C~85°C	−7.25	-	7.25	
	t_{HSICLK_START}	Start-up Time	T_A=−40°C~85°C, the oscillator frequency remains +/−3% of the nominal frequency or triggers a power-on reset.	-	-	4	ms
LSICLK	f_{LSICLK}	Operating frequency	-	-	65.536	-	kHz
	f_{LSICLK_DRIFT}	Frequency drift	T_A=−20°C~65°C	−2.7	-	1	%
			T_A=−40°C~85°C	−8.65	-	6.1	

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.11 Voltage Reference1（REF1）

Table 14 Voltage Reference1[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REF1}	Internal reference voltage[2]	-	0.486	0.501	0.519	V
V_{REF1_DRIFT}	Internal reference voltage drift	T_A=–40°C to 85°C	−80	-	80	PPM/C

Note:

[1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

[2] Used for low dropout linear regulators (LDO) and other IP modules.

5.12 Voltage Reference2（REF2）

Table 15 Voltage Reference2[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REF2}	Internal reference voltage[2]	-	1.2	1.21	1.22	V
V_{REF2_DRIFT}	Internal reference voltage drift	T_A=–40°C to 85°C	−20	-	20	PPM/°C

Note:

[1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

[2] It is used for C-ADC and V-ADC.

5.13 Flash Memory

Table 16 Flash Memory[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
-	Data retention	-	20	100	-	Years
-	Flash programming write cycle	Data Flash	-	100000	-	Cycles
		Instruction Flash	-	100000	-	
$t_{ROWPROG}$	Row programming time	-	-	-	150	μs
$t_{MASSERASE}$	Block erase time	T_A=–40°C to 85°C	-	-	40	ms
$t_{SECTORERASE}$	Sector erase time	T_A=–40°C to 85°C	-	-	3	
$I_{FLASHREAD}$	Flash read current	T_A=–40°C to 85°C	-	0.2	0.4	mA
$I_{FLASHWRTIE}$	Flash write current	T_A=–40°C to 85°C	-	-	2	
$I_{FLASHERASE}$	Flash erase current	T_A=–40°C to 85°C	-	-	1.5	

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.14 Internal Temperature Sensor

Table 17 Internal Temperature Sensor[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{TEMP}	Internal temperature sensor voltage drift	V_{TEMPP}	1.84	1.97	2	mV/°C
		V_{TEMPP}–V_{TEMPN} （Guaranteed by design)	0.17	0.18	0.19	

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.15 NTC Thermistor Measurement

Table 18 NTC Thermistor Measurement[1]

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$R_{NTRC(PU)}$	Internal pull-up resistor	12	15	18	kΩ
$R_{NTC(DRIFT)}$	Resistance drift with temperature changes	–250	–120	0	PPM/°C

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.16 C-ADC

Table 19 C-ADC[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{C-ADC_IN}	Input voltage range	-	–0.1	-	0.1	V
t_{C-ADC_CONV}	Conversion time	Single conversion	-	1000	-	ms
V_{reso}	Quantization accuracy	1 LSB	-	3.6	-	μV
INL	Integral nonlinearity	16 bits, optimal input voltage range	–20.5	3.1	20.5	LSB
DNL	Differential nonlinearity	16 bits, no missing codes	-	1.4	-	
V_{offset}	Offset error	16 bits, post calibration	–2.42	1.4	2.42	
V_{offset_drift}	Offset error drift	15 bits + (MSB) 1 bit sign, post calibration	-	0.029	-	LSB/°C

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
E_g	Gain error	15 bits + (MSB) 1 bit sign, covering input voltage range	–274	84	274	LSB
E_{g_drift}	Gain error drift	15 bits + (MSB) 1 bit sign, covering input voltage range	-	3.32	-	LSB/°C
R_{in}	Effective input resistance	-	7	-	-	MΩ

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.17 V-ADC

Table 20 V-ADC[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{V\text{-}ADC\_TS\_GPIO}$	Input voltage range	$V_{FS}=V_{REF2}$	–0.2	-	1.2	V
V_{BAT_MODE}	Battery input voltage	-	–0.2	-	5.4	
INL	Integral nonlinearity	16 bits, optimal fit, –0.1V to 0.8xV_{REF2}	–7.5	3.4	7.5	LSB
DNL	Differential nonlinearity	16 bits, no missing codes	-	1.38	-	
V_{offset}	Offset error	16 bits, post calibration[2], $V_{FS}=V_{REF2}$	–3.9	1.02	3.9	
V_{offset_drift}	Offset error drift	16 bits, post calibration[2], $V_{FS}=V_{REF2}$			0.047	LSB/°C
E_g	Gain error	16 bits, –0.1V to 0.8xV_{FS}	–3	48	368	LSB
E_{g_drift}	Gain error drift	16 bits, –0.1V to 0.8xV_{FS}	-	-	3.5	LSB/°C
R_{in}	Effective input resistance	-	8	-	-	MΩ
$t_{V\text{-}ADC\_CONV}$	Conversion time	OSR=128	-	15.4	-	ms
		OSR=256	-	31	-	
		OSR=512	-	61.4	-	
ENOB	Effective number of bits	-	14	16	-	bits

Note:

[1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

[2] Factory calibration.

5.18 I2C I/O

Table 21 I2C I/O[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IH}	High-level input voltage	SCL, SDA, V_{LDO}=1.5V	1.39	-	-	V
V_{IL}	Low-level input voltage	V_{LDO}=1.5V	-	-	0.41	
V_{OL}	Low-level output voltage	I_{OL}=1 mA, V_{LDO}=1.5V	-	-	0.36	
C_I	Input capacitance	-	-	-	10	pF
I_{lkg}	Input leakage current	-	-	1	-	μA

Note: [1] Unless otherwise specified, data is recorded under conditions of TA = –40°C to 85°C.

5.19 I2C Timing (100kHz)

Table 22 I2C Timing (100kHz)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{SCL}	Clock operating frequency	SCL duty cycle is 50%	-	-	100	kHz
$t_{HD:STA}$	START condition hold time	-	4.0	-	-	μs
t_{LOW}	Low period of the SCL clock	-	4.7	-	-	
t_{HIGH}	High period of the SCL clock	-	4.0	-	-	
$t_{SU:STA}$	Repeated START setup	-	4.7	-	-	
$t_{HD:DAT}$	Data hold time (SDA input)	-	0	-	-	ns
$t_{SU:DAT}$	Data setup time (SDA input)	-	250	-	-	
t_r	Clock rise time	10%~90%	-	-	1000	
t_f	Clock fall time	90%~10%	-	-	300	
$t_{SU:STO}$	STOP condition setup time	-	4.0	-	-	μs
t_{BUF}	Bus free time between STOP and START	-	4.7	-	-	

5.20 I2C Timing (400kHz)

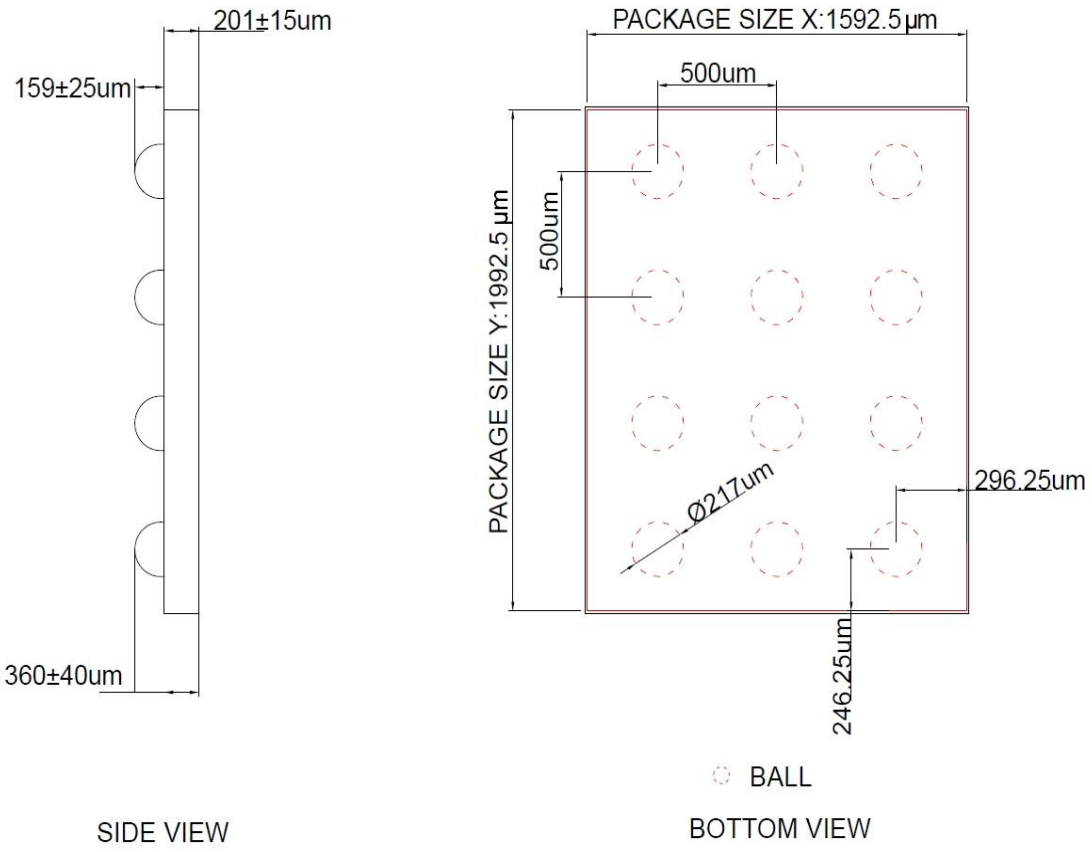
Table 23 I2C Timing (400kHz)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{SCL}	Clock operating frequency	SCL duty cycle is 50%	-	-	400	kHz
$t_{HD:STA}$	START condition hold time	-	0.6	-	-	μs
t_{LOW}	Low period of the SCL clock	-	1.3	-	-	
t_{HIGH}	High period of the SCL clock	-	600	-	-	ns
$t_{SU:STA}$	Repeated START setup	-	600	-	-	
$t_{HD:DAT}$	Data hold time (SDA input)	-	0	-	-	
$t_{SU:DAT}$	Data setup time (SDA input)	-	250	-	-	
t_r	Clock rise time	10%~90%	-	-	300	
t_f	Clock fall time	90%~10%	-	-	300	
$t_{SU:STO}$	STOP condition setup time	-	0.6	-	-	μs
t_{BUF}	Bus free time between STOP and START	-	1.3	-	-	

6 Package Information

6.1 WLCSP12 Package Information

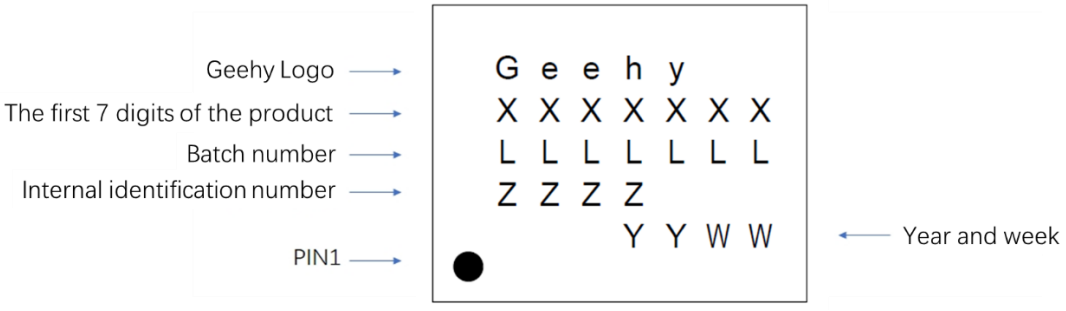
Figure 8 WLCSP12 Package Diagram



（1） The figure is not drawn to scale.

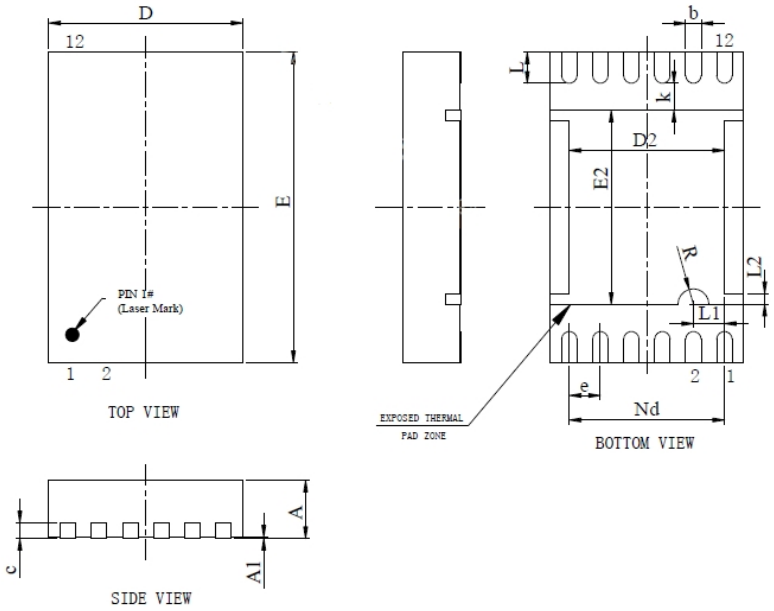
（2） All pins should be soldered to the PCB.

Figure 9 WLCSP12 Package Identification



6.2 DFN12 Package Information

Figure 10 DFN12 Package Diagram

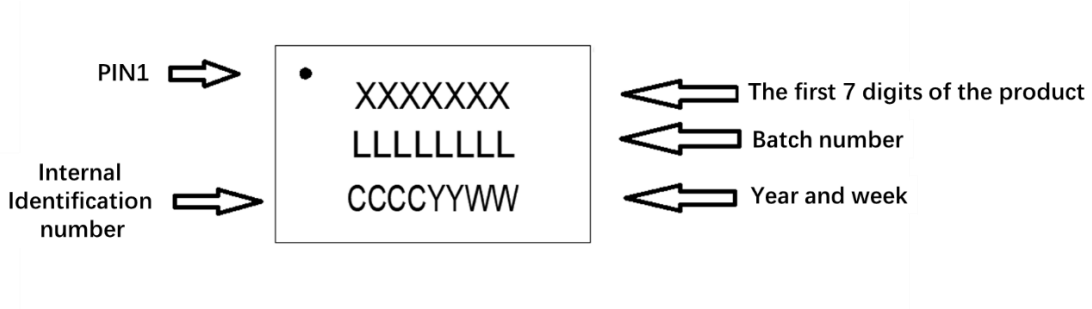


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.203REF		
D	2.40	2.50	2.60
D2	1.90	2.00	2.10
e	0.40BSC		
Nd	2.00BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
R	0.15	0.20	0.25
K	0.35REF		
L1	0.40REF		
L2	0.14REF		

（1） The figure is not drawn to scale.

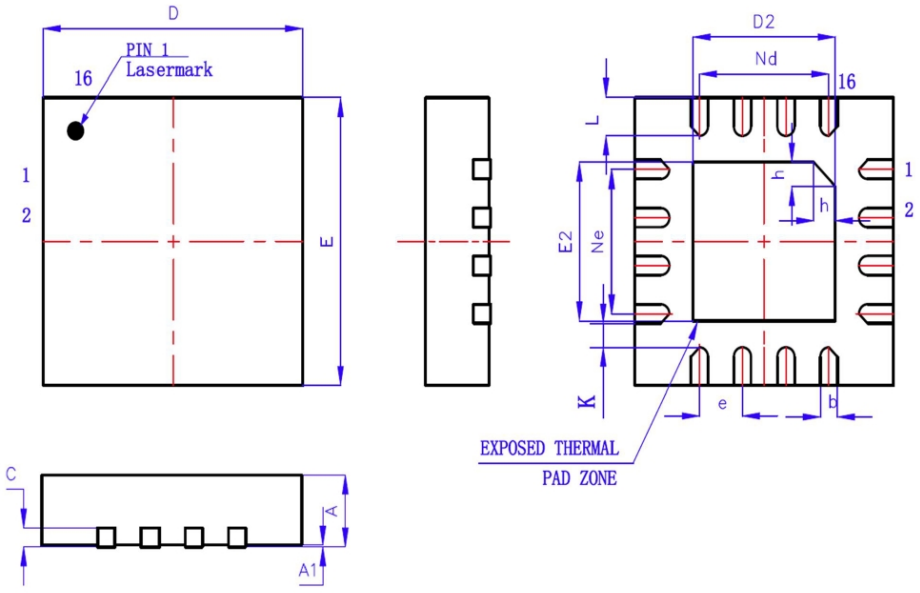
（2） All pins should be soldered to the PCB.

Figure 11 DFN12 Package Identification



1.1 QFN16 Package Information

Figure 12 QFN16 Package Diagram

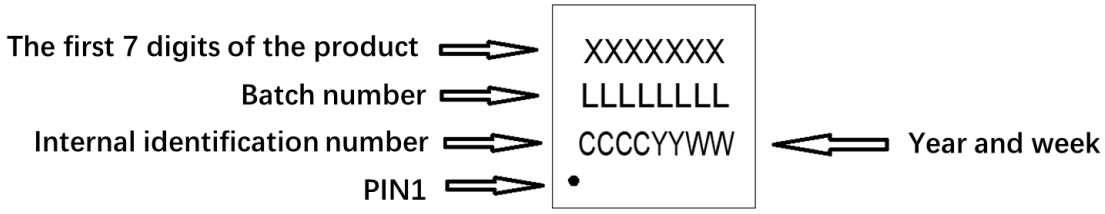


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.20	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
Ne	1.50BSC		
L	0.25	0.30	0.35
K	0.20	-	-
h	0.30	0.35	0.40
L/F载体尺寸	82*82		

（1） The figure is not drawn to scale.

（2） All pins should be soldered to the PCB.

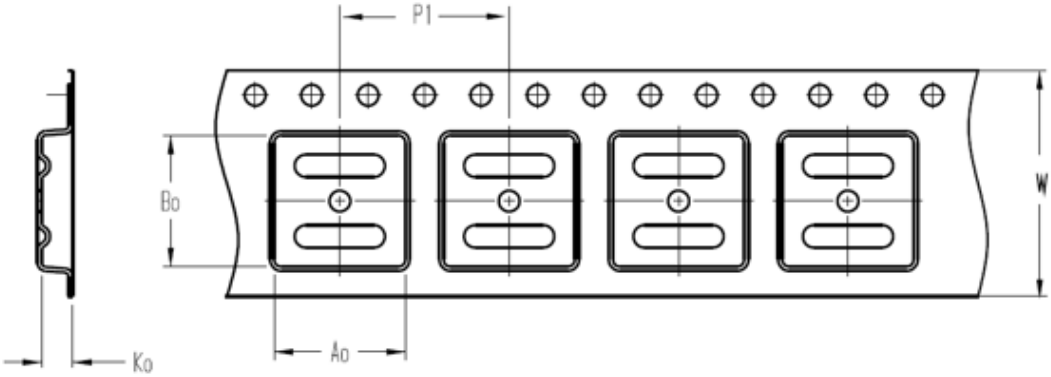
Figure 13 QFN16 Package Identification



7 Packaging Information

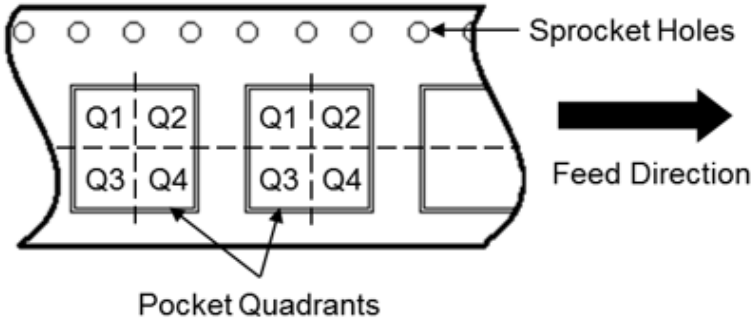
Figure 14 Reel Packaging Specification Drawing

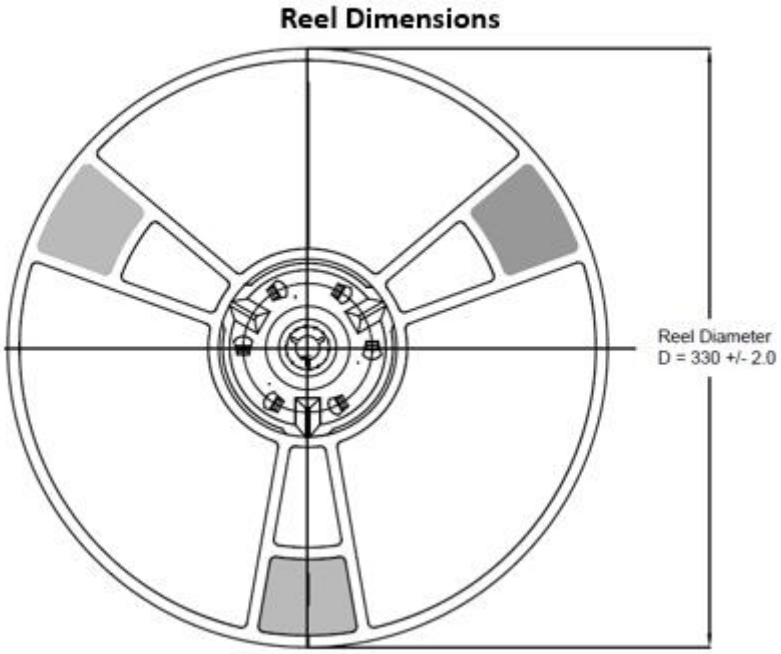
Tape Dimensions



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Quadrant Assignments For PIN1 Orientation In Tape





All photos are for reference only, and the appearance is subject to the product.

Table 24 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	Reel Diameter（inch）	A0（mm）	B0（mm）	P1（mm）	K0（mm）	W（mm）	Pin1 Quadrant
BMP561Y8Y6	WLCSP	12	3000	7	1.75	2.15	4	0.55	8	Q1
BMP561Y8D6	DFN	12	6000	13	2.70	4.20	8.00	1.10	12.00	Q3
BMP561L8U6	QFN	16	5000	13	3.25	3.25	8.00	1.10	12.00	Q1

8 Ordering Information

Figure 15 Product Information Naming Rules

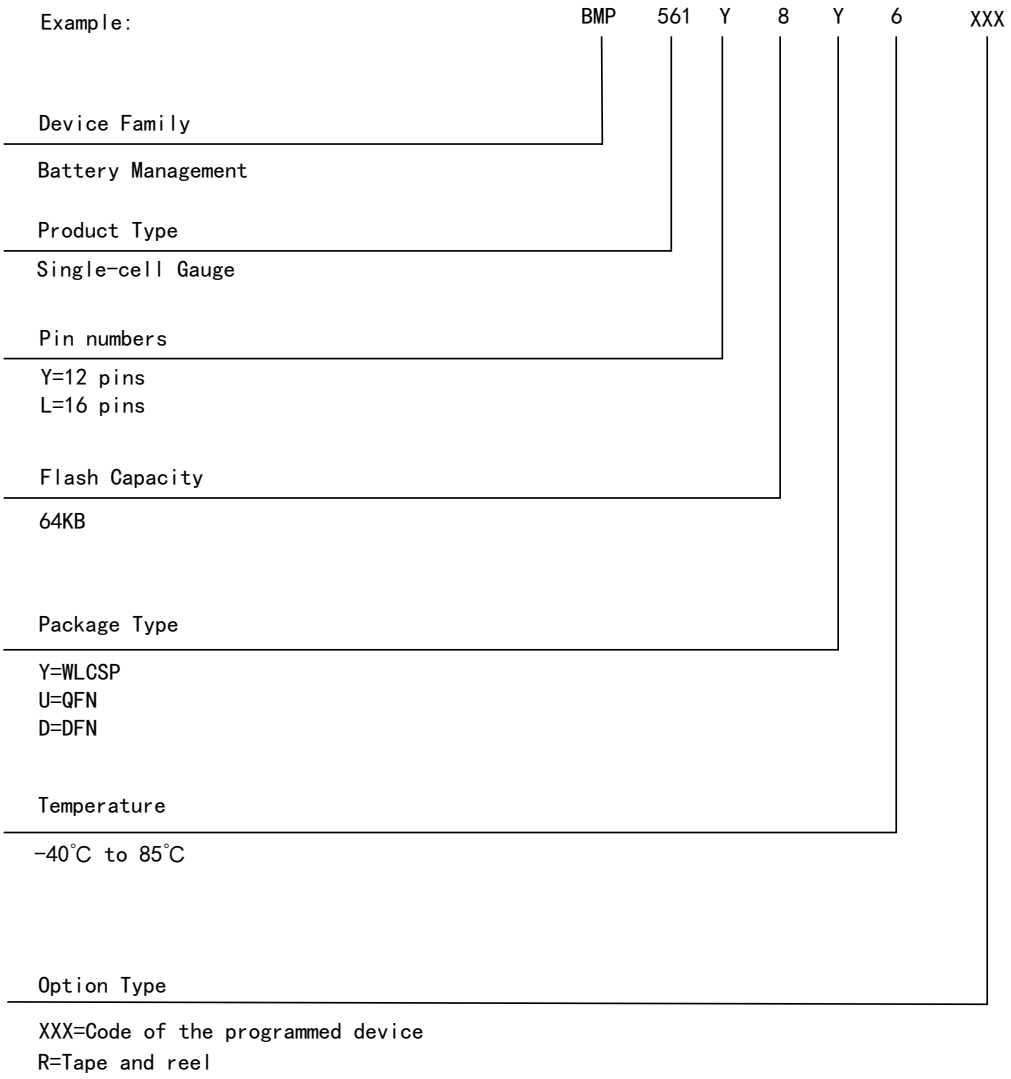


Table 25 Ordering Information Table

Order Code	Main FLASH (KB)	Data FLASH (KB)	SRAM (KB)	Package	SPQ	Temperature Range
BMP561Y8Y6	64	4	8	WLCSP12	3000	-40°C ~85°C
BMP561Y8D6	64	4	8	DFN12	6000	-40°C ~85°C
BMP561L8U6	64	4	8	QFN16	5000	-40°C ~85°C

Note: SPQ=Smallest Packaging Quantity.

9 Commonly Used Function Module Denomination

Table 26 Commonly Used Function Module Denomination

Full name	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
External Interrupt	EINT
General-purpose IO	GPIO
Wake-up controller	WUPT
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
Power management unit	PMU
Analog-to-digital converter	ADC
I2C Interface	I2C
Universal asynchronous transmitter receiver	UART
Flash interface controller unit	FMC
Hash algorithm	SHA

10 Revision History

Table 27 Document Revision History

Date	Version	Revision History
February 2025	1.0	• Initial release
January 2026	1.1	• Refined the device name in Table 25 of Packaging Information • Corrected the start addresses of SYSCTRL and FLASH in the address mapping table.
June 2026	1.2	• Remove all HSC-related content from the document.

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